CLAIMS

We claim:

1. A method for detecting over programming in a memory system that uses multiple logical pages, comprising the steps of:

programming a first multi-state storage element with data for a particular logical page; and

using data from a logical page different than said particular logical page to determine whether said step of programming said first multi-state storage element over programmed said multi-state storage element.

2. A method according to claim 1, further comprising the step of:

programming said first multi-state storage element with data for said logical page different than said particular logical page prior to programming said first multi-state storage element with data for said particular logical page.

3. A method according to claim 2, wherein said step of using data includes the steps of:

determining whether a threshold voltage of said first multi-state storage element is greater than a compare value; and

determining that said first multi-state storage element is over programmed if said threshold voltage of said first multi-state storage element is greater than said compare value and data for said logical page indicates that said threshold voltage of said first multi-state storage element should not be greater than said compare value.

4. A method according to claim 3, wherein:

said first multi-state storage element is capable of storing at least two bits of data in at least four states including state 0, state 1, state 2 and state 3;

a first bit of said two bits of data is for said particular logical page;

a second bit of said two bits of data is for said logical page different than said particular logical page;

said first bit is programmed in state 2 and state 3;

said second bit is programmed in state 1 and state 2;

said compare value is between state 2 and state 3; and

said data for said logical page different than said particular page indicates that said threshold voltage of said first multi-state storage element should not be greater than said compare value if said second bit is programmed such that said first multi-state storage element should be in state 2.

5. A method according to claim 1, wherein said step of using data includes the steps of:

performing a verify operation to determine a threshold voltage for said first multi-state storage element; and

using said data from said logical page different than said particular logical page to determine whether said threshold voltage should be above said first compare point.

6. A method according to claim 1, wherein:

said first multi-state storage element is capable of storing multiple bits of data in multiple states;

a first bit of said multiple bits of data is for said particular logical page;

a second bit of said multiple bits of data is for said logical page different than said

particular logical page; and

said step of using data includes determining whether said step of programming said first multi-state storage element with data for said particular logical page intended to program said first multi-state storage element into a first state but programmed said first multi-state storage element beyond said first state.

7. A method according to claim 6, further comprising the step of:

determining whether said first multi-state storage element was programmed beyond a second state after said step of using data.

8. A method according to claim 7, further comprising the steps of:

programming said first multi-state storage element with data for said logical page different than said particular logical page prior to programming said first multi-state storage element with data for said particular logical page, said particular logical page is an upper page, said logical page different than said particular logical page is a lower page; and

determining whether said first multi-state storage element was programmed beyond a third state in response to said step of programming said first multi-state storage element with data for said logical page different than said particular logical page, said third state is associated with programming said second bit, said steps of using and determining whether said first multi-state storage element was programmed beyond a second state are performed in response to said step of programming a first multi-state storage element with data for a particular logical page.

9. A method according to claim 1, further comprising the step of:

programming a second multi-state storage element subsequent to programming said first multi-state storage element and prior to said step of using, said first multi-state

storage is connected to a first word line and said first multi-state storage is connected to a second word line.

10. A method according to claim 1, wherein:

said first multi-state storage element stores data using multiple states arranges according to a gray code.

11. A method according to claim 1, wherein:

said step of programming and using data are performed by a state machine.

12. A method according to claim 1, wherein:

said first multi-state storage element is part of an array of storage elements;

said array of storage elements is on an integrated circuit chip;

said step of programming and using data are performed by a state machine; and

said state machine is on said integrated circuit chip.

13. A method according to claim 1, wherein:

said first multi-state storage element is part of an array of storage elements;

said array of storage elements is on an integrated circuit chip;

said memory system includes a controller;

said controlled is not on said integrated circuit chip;

said step of programming and using data are performed by a state machine; and

said state machine is on said integrated circuit chip.

14. A method according to claim 1, wherein:

said first multi-state storage element is part of an array of storage elements;

said array of storage elements is on an integrated circuit chip; and

said step of programming and using data are performed by circuits on said integrated circuit chip.

15. A method according to claim 1, wherein:

said first multi-state storage element is part of an array of storage elements;

said step of programming is performed in response to an instruction from a host system in communication with said array of storage elements; and

said array of storage elements are removable from said host system.

16. A method according to claim 1, wherein:

said first multi-state storage element is a flash memory element.

17. A method according to claim 1, wherein:

said first multi-state storage element is a NAND flash memory element.

18. A method for detecting over programming in a memory system that uses multiple logical pages, comprising the steps of:

determining whether a threshold voltage of a first multi-state storage element is greater than a compare value, said first multi-state storage element stores information for at least a first logical page and a second logical page, said step of determining whether said threshold voltage of said first multi-state storage element is greater than said compare value is performed after writing data to said second logical page; and

determining whether said first multi-state storage element is over programmed based on data from said first logical page and said step of determining whether a threshold voltage of a first multi-state storage element is greater than a compare value.

19. A method according to claim 18, wherein:

said first multi-state storage element stores data using multiple states;

at least a first state and a second state of said multiple states are associated with programming data for said second logical page;

said data from said first logical page is stored in said first multi-state storage element;

said data from said first logical page indicates which of said first state or said second said first multi-state storage element should be in; and

said first multi-state storage element is over programmed if said first multi-state storage element should be in said first state but has been programmed beyond said first state.

20. A method according to claim 18, wherein:

said first multi-state storage element is part of an array of storage elements;

said array of storage elements is on an integrated circuit chip; and

said steps of determining whether a threshold voltage of a first multi-state storage element is greater than a compare value and determining whether said first multi-state storage element is over programmed are performed by one or more circuits on said integrated circuit chip.

21. A method according to claim 18, wherein:

said first multi-state storage element is a NAND flash memory element.

22. A memory system, comprising:

an array of storage elements; and

a managing circuit in communication with said array of storage elements, said managing circuit performs programming operations including programming a first multi-state storage element with data for a particular logical page, said managing circuit also

performs over programming detection including using data from a logical page different than said particular logical page to determine whether said programming of said first multi-state storage element with data for said particular logical page over programmed said first multi-state storage element.

23. A memory system according to claim 22, wherein:
said managing circuit includes a state machine.

24. A memory system according to claim 23, further comprising:
a controller, said state machine and said array of storage elements are on a first integrated circuit chip and said controller is not on said first integrated circuit chip.

25. A memory system according to claim 24, wherein:
said state machine performs said over programming detection.

26. A memory system according to claim 23, wherein:
said managing circuit further programs said first multi-state storage element with said data for said logical page different than said particular logical page prior to programming said first multi-state storage element with data for said particular logical page.

27. A memory system according to claim 26, wherein:
said managing circuit performs said over programming detection by determining whether a threshold voltage of said first multi-state storage element is greater than a compare value and determining that said first multi-state storage element is over programmed if said threshold voltage of said first multi-state storage element is greater than said compare value and data for said logical page indicates that said threshold

voltage of said first multi-state storage element should not be greater than said compare value.

28. A memory system using multiple logical pages, comprising:

means for programming a first multi-state storage element with data for a particular logical page; and

means for using data from a logical page different than said particular logical page to determine whether said first multi-state storage element is over programmed.

29. A memory system according to claim 28, further comprising:

means for programming a second multi-state storage element subsequent to programming said first multi-state storage element and prior to said step of using, said first multi-state storage connected to a control line and said second multi-state storage connected to a control line.

30. A memory system according to claim 29, wherein:

said first multi-state storage element is a NAND flash memory element.